Monolithic 2–18 GHz Low Loss, On-Chip Biased PIN Diode Switches

Jar-Lon Lee, *Senior Member, IEEE*, Donna Zych, Elias Reese, and Denis M. Drury, *Senior Member, IEEE*

Abstract— **Two state-of-the-art monolithic GaAs PIN diode switches have been designed, fabricated and tested. These single-pole double-throw (SPDT) switches exhibit insertion losses of 1.15 ± 0.15 dB over a 2–18 GHz band, which is an unprecedented performance in loss and flatness for monolithic wideband switches incorporating on-chip bias networks. Isolation and return loss are greater than 43 dB and 12 dB, respectively, and the input port power handling is 23 dBm at 1-dB insertion loss compression. These performance characteristics were measured at a nominal bias setting of −8 V, which corresponds to 3.7 mA of series diode bias current and a total dc power consumption of 55mW. The input power at the third-order interception is 40 dBm. The switches can handle up to 31 dBm (1.25 W) at a higher bias of −18 V and 9.3 mA.**

I. Introduction

MONOLITHIC GaAs PIN diodes have been successfully demonstrated as control elements in many monolithic microwave integrated circuits (MMICs), including attenuators/limiters [1], [2], phase shifters [3] and switches [4], [5]. These components are widely used in applications such as transmit/receive modules, multiplexers/de-multiplexers, channelized-amplifiers, and sampling/hold units, where a wide bandwidth and low loss are required.

Both GaAs MESFET's and vertical PIN diodes have shown success in broadband microwave switch applications [6], [7]. However, the PIN diode, with its low resistance and capacitance, demonstrates a much higher cutoff frequency (900–1000 GHz versus typical MESFET's 300 GHz) [4], [8]. Unlike the MESFET switches [6], [9], the third-order interception point of the PIN diode switches increases with the frequency, as will be shown later in the measurement section. Other advantages of the PIN diode are its small size, low loss and high breakdown voltage [2], [8]. Although PIN diode switches with off-chip bias are reported to have insertion losses as low as 0.4–1 dB over 0.1–20 GHz [5], the switches with on-chip bias currently demonstrate an insertion loss of nearly 2 dB. Furthermore, the resultant bandwidth of devices using an off-chip bias network is directly affected by the network implementation.

This paper describes two versions of an improved 2–18 GHz GaAs monolithic single-pole double-throw (SPDT) PIN diode switch using on-chip bias networks. The version A topology uses a common cathode connection on the shunt diodes, while version B uses a common anode connection. The fabrication of the switches, the characteristics of the PIN diodes and the performance of the switches are discussed.

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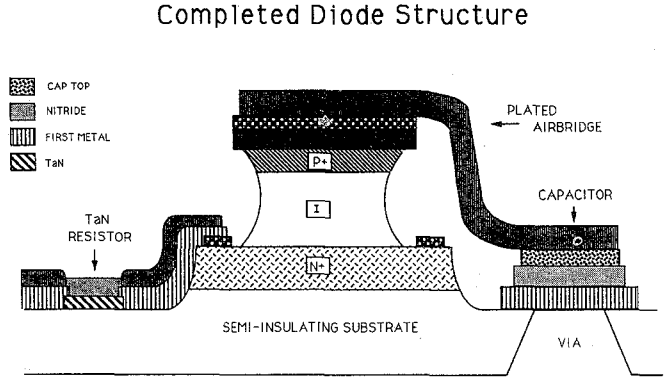


Fig.1. Schematic of vertical PIN Diode cross-section.

II. GaAs Vertical Pin Diode

The vertical 18-micron-diameter PIN diode was optical-lithographically defined on metal organic chemical vapor deposition (MOCVD) grown epitaxial layers. A dry etch was used to etch through to the I/N+ interface, as depicted in Fig. 1. The cathode contacts on top of the N+ layer were self-aligned to the P+ layer, followed by wet etching of the N+ layer to isolate the 3.5-micron-thick diode structure. The resulting PIN diode was then protected by a photo-resist which remained in place during all subsequent fabrication steps. This GaAs MMIC PIN diode production process on the 3-inch-diameter substrate has demonstrated a dc yield of over 90% [8].

The PIN diode was characterized and modeled by using on-wafer rf probe data. The dc measurements, along with rf data analysis involving s- and h-parameters over the 0.05–18 GHz frequency range, were used to model the PIN diode in forward bias as shown in Fig. 2. The topology of the model is adopted from the EEsof™ Element Catalog [10], and the parameters are optimized to fit the measured data. The diode junction capacitance (C_j) is 70–80 pF. The resistance R_j exhibits a dc gradient of 20 (mV)/I_f(mA) , and the series resistance (R_f) has a gradient of 13 (mV)/I_f(mA), whereI_f is the forward bias current. A parasitic resistance (R_p) of 2 ohm is associated with the diode leads.R_j accounts for the junction resistance at the P-I interface of the PIN diode, similar to a traditional P-N junction. At dc and low frequencies, R_j is the dominant resistance in the PIN diode. The series resistance R_f originates from the carrier recombination in the bulk I-region of the PIN diode. At higher frequencies, the resistance of this

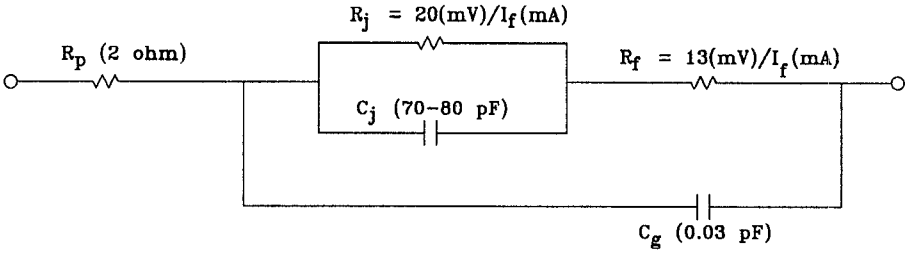


Fig. 2. Vertical PIN Diode model for 0.05–18 GHz as function of the dc forward bias current I_f.

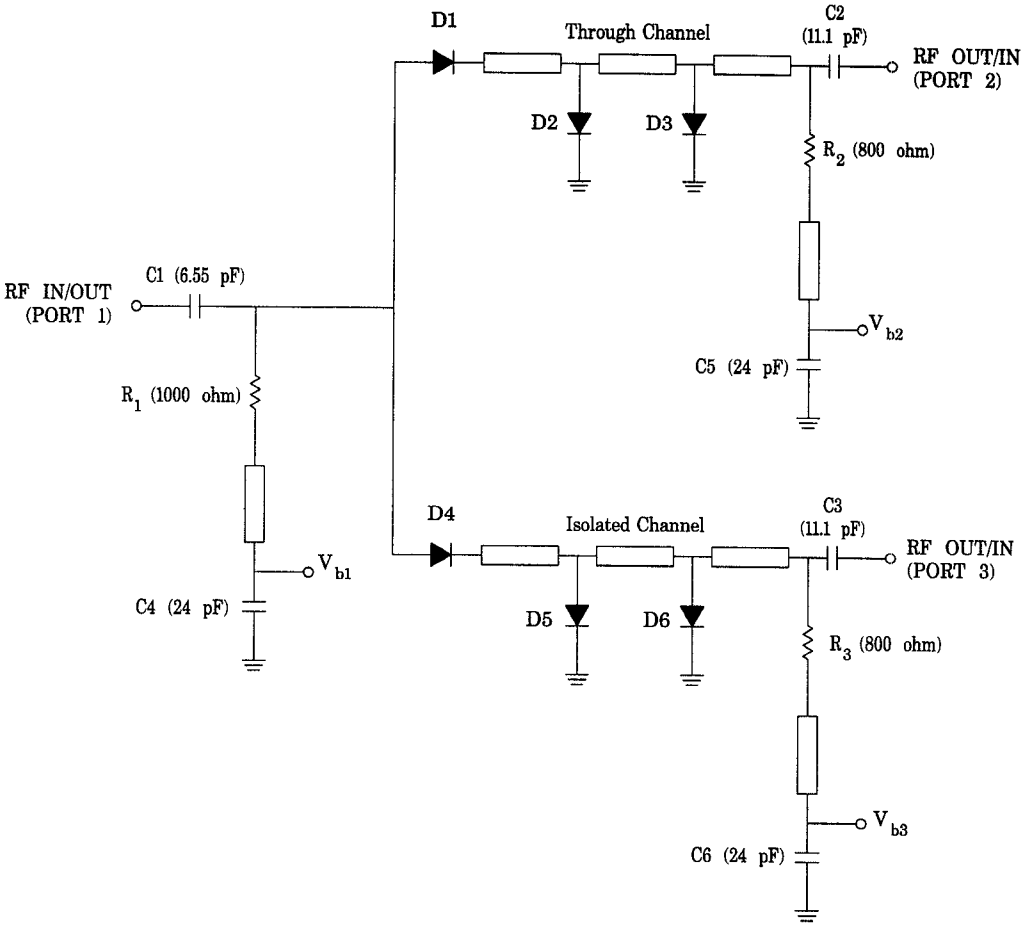


Fig. 3(a). Schematic of a SPDT PIN diode switch: version A with a P-I-N-via configuration.

bulk level recombination is more significant than the junction resistanceR_j, since the junction capacitor "shorts out."

When the diode was reverse biased, a very small reverse current was seen and a highly capacitive impedance was observed. In effect R_j andR_f become open and the resulting dominant diode elements at reverse bias are a 0.03-pF gap capacitance (C_g) in series with the resistance R_p.

The minimum forward bias current ranges typically from 2 to 5 mA for this PIN switch. Typical reverse breakdown is 35 V at 10 μA [8], making the PIN diode superior to MESFET's in high-power applications. The PIN diode, when grounded through a via, is often aligned in a P-I-N-via orientation. The version A switch was designed according to this structure. An N-I- P-via oriented structure (version B switch, to be discussed later) was also included in the design as an option of opposite bias palarity.

III. Circuit Design – Version A

The circuit schematic of the on-chip biased SPDT PIN diode switch, version A, is shown in Fig. 3(a). Two approaches were considered for biasing the diodes. A spiral inductor employed as an on-chip rf choke was an attractive option due to its relatively low loss. However, resistive bias networks were favored as a better choice for their advantages of: 1) higher modeling accuracy, which corresponds to more predictable responses; 2) wider operation bandwidth; and 3) smaller size. Referring to Fig. 3(a), a "through" channel (Port 1 to Port 2) is formed

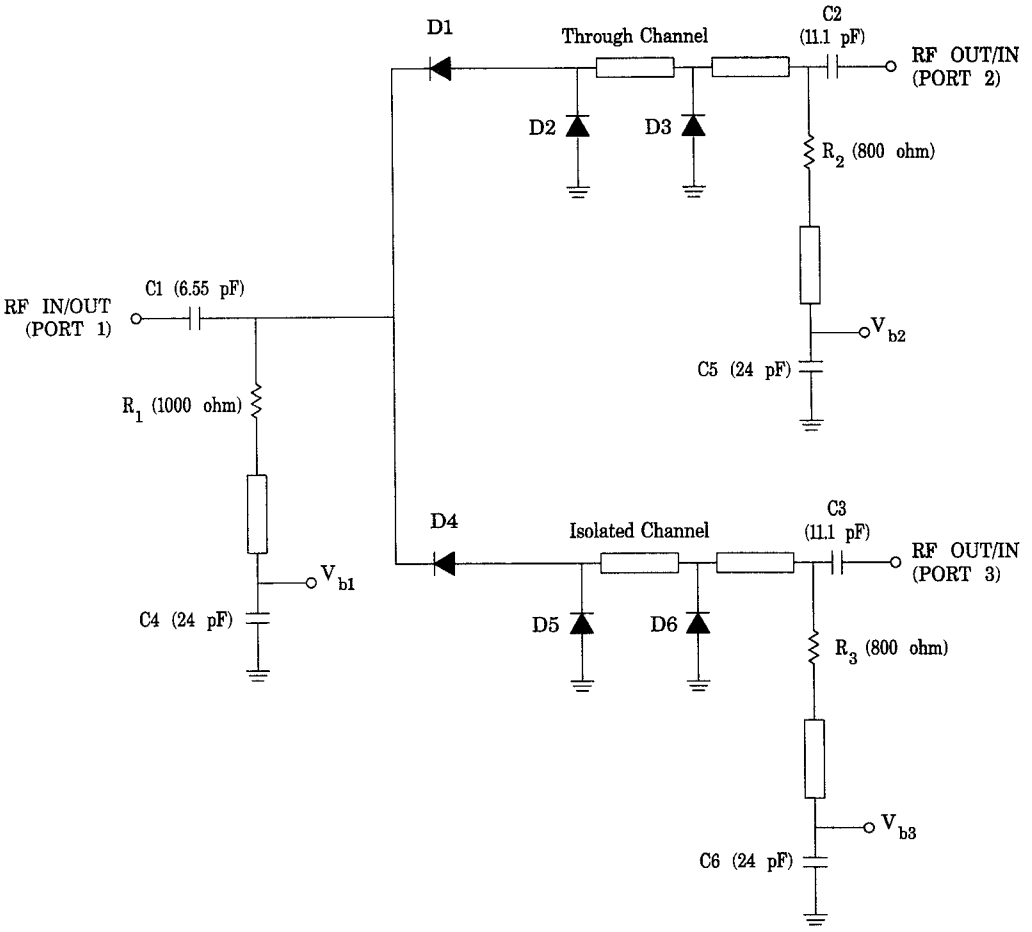


Fig. 3(b). Schematic of a SPDT PIN diode switch: version B with an N-I-P-via configuration.

when the shunt diodes D2 and D3 are reverse biased (OFF) by a negative voltage V_{b2} while the series diode D1 is forward biased (ON). Similarly, a positive voltage V_{b3} applied to Port 3 forward biases diodes D5 and D6, and reverse biases diode D4. This forms an "isolated" channel from Port 1 to Port 3.

A. Through Channel

In the through path, the series PIN diode typically contributes 0.3 to 0.8 dB of insertion loss depending upon the bias current. The critical part in controlling the total loss of the switch is to minimize the rf signal leakage in the shunt bias networks over a wide frequency range (2–18 GHz). A lower leakage level can be achieved by raising the bias resistances R_1 and R_2 as shown in Fig. 3(a), which also results in a lower dc current through the resistive bias networks. However, the penalty for this reduced rf leakage is a higher loss in the series PIN diode due to the lower dc current. Thus some compromise is necessary to trade off the series and shunt losses in the through channel to reach a minimum insertion loss across a wide frequency range.

The dc current I_{f1} on the series PIN diode ranges from 2–8 mA and is given by

$$I_{f1} = \frac{V_{b12} - V_f}{R_1 + R_2} \tag{1}$$

where $V_{b12} = V_{b1} - V_{b2}$; and $V_f = 1.3$ V is the turn-on voltage of the PIN diode D1 (Fig. 3(a)). The current dependence of R_j (junction resistance), and R_f (forward bias resistance) of the series PIN diode D1 can be expressed in terms of R_1 and R_2 as

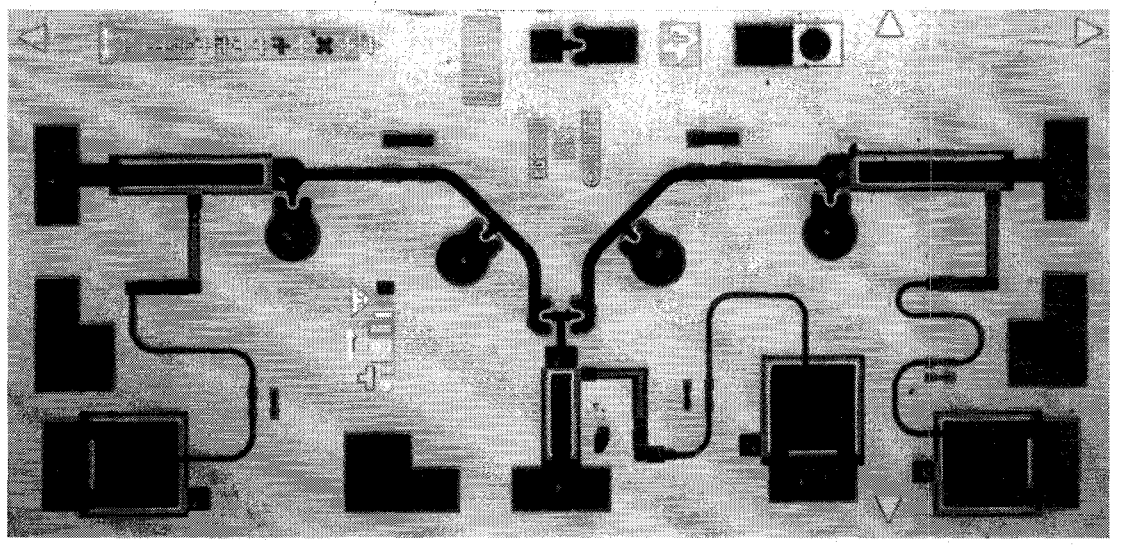
$$R_j = \frac{45(mV)}{v_{b12} - V_f} \quad (R_1 + R_2). \tag{2}$$

$$R_f = \frac{2(mV)}{V_{b12} - V_f}(R_1 + R_2). \tag{3}$$

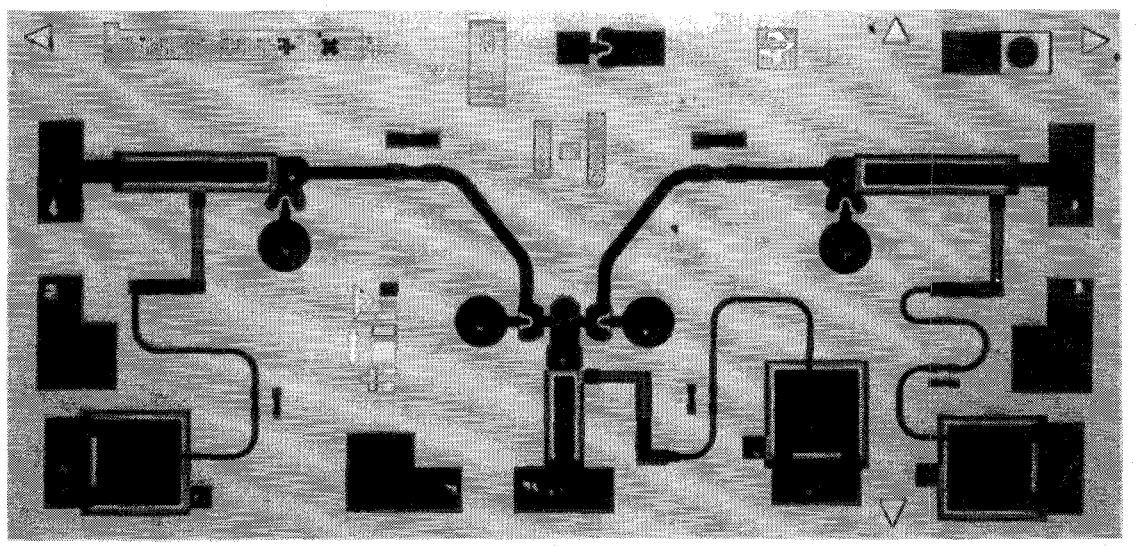
These bias resistors R_1 and R_2 control not only the rf series loss through R_j and R_f in the PIN diode, but also the rf shunt loss in the bias networks.

The shunt loss in the bias network was reduced by using high resistor values ($R1 = 1000$ ohm and $R2 = 800$ ohm), plus an 85-ohm transmission line inserted between these resistors and the shunt bypass capacitors (C4 and C5 in Fig. 3(a)). These transformation lines suppressed the rf shunt loss in the bias networks, reducing the through channel insertion loss by 0.3 dB at high frequencies, and extended the operating band to 19 GHz. Bias networks as a whole contributed about 0.25-dB loss at the input, and 0.25-dB loss at the output.

To precisely control the highband cutoff, which was sensitively dictated by the effective lengths of the signal paths and the associated bias lines, all microstrip bends in the circuit were designed using an empirical formula. The formula for the equivalent path length of a microstrip radial bend adopts as the radius of curvature the summation of the bend's inner radius and a third of the bend's width, rather than a half of the



(a)



(b)

Fig. 4. (a) Layout of the SPDT PIN diode switch: version A. (b) Layout of the SPDT PIN diode switch: version B.

bend's width as conventionally used. Increasing the input and output capacitances (C_1 and C_2) would damage the highband insertion loss although the lowband return losses are improved. A combination of $C_1 = 6.55$ pF and $C_2 = 11.1$ pF produced a best balance between the insertion loss level and the high frequency cutoff.

The interface model for both switch designs included a pair of 0.030-inch bondwires (0.001 inch diameter), which represents 0.4 nH of inductance, and a transmission line flare of 0.0245 × 0.009 inch on a 0.010-inch-thick alumina substrate to simulate the rf input and output interconnects. Proper simulation of the bondwire inductance was critical to achieve low loss performance. The flares on both MMIC and the thin film networks (TFN's) were designed to match the bondwire inductance from dc to 24 GHz.

B. Isolated Channel

In the isolated path, the reverse-biased diode D4 and the forward-biased diodes D5 and D6 provided an isolation of 40–60 dB. A quarter-wave transformation between D5 and D6 becomes less important in sustaining a high isolation if the reverse-biased PIN diode D4 exhibits a sufficiently high impedance. This impedance depends upon the small diode gap capacitance (Cg) (Fig. 2).

Furthermore, when the series PIN diode D4 presents a high impedance in the reverse bias state, the location of the first shunt diode D5 becomes more flexible. The resultant layout of the version A switch is shown in Fig. 4(a), where the diode D5 has been moved 10 mil away from the series PIN diode D4 so that the insertion loss of the through channel is slightly improved (by about 0.1 dB at 19 GHz) at the expense of degrading the isolation by 1 dB only.

Nominal bias voltages of $V_{b2} = -8$ V (3.7 mA) and $V_{b3} = +5$ V (4.6 mA) were chosen for the through channel and the isolated channel, respectively, with $V_{b1} = 0$ V. The through channel loss prediction was 1.0 ± 0.1 dB over 2–18 GHz, with minimum input and output return losses of 12 dB. A more negative V_{b2} would achieve a lower insertion loss and a higher rf power handling capability.

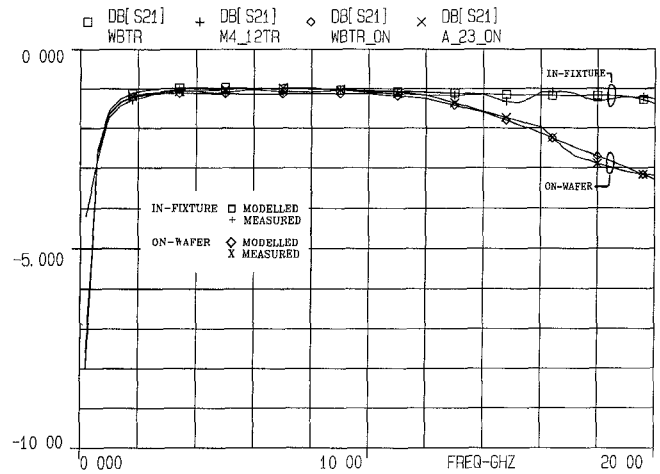


Fig. 5. Insertion loss of a SPDT PIN diode switch (bias current = 3.7 mA).

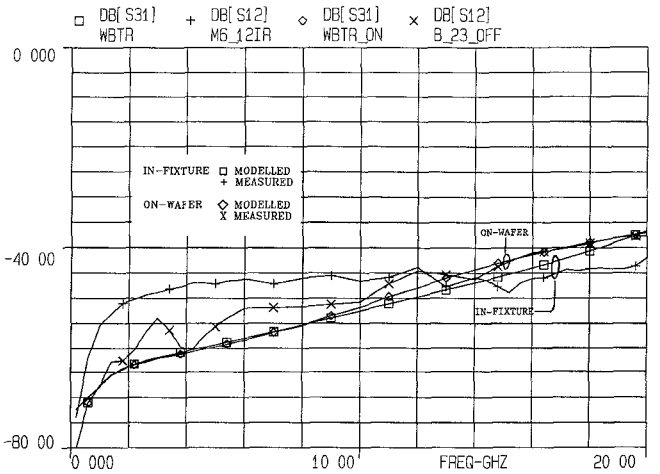


Fig. 6. Isolation of a SPDT PIN diode switch (bias current = 3.7 mA).

IV. Circuit Design—Version B

A version B switch was designed to provide microwave module designers another bias option. Version B, shown in Fig. 3(b), has all six diodes reversed in polarity compared to switch A. All the design techniques previously discussed have also been used to generate version B of the PIN diode switch. The bias polarity must now change to $V_{b2} = +8$ V (3.7 mA) and $V_{b3} = -5$ V (4.6 mA) for the same channel designation to be preserved. The layout of version B is shown in Fig. 4(b). Predicted insertion loss of the through channel was 1.0 ± 0.09 dB over the 2–18 GHz frequency range. The minimum input and output return losses were 13 dB. Due to structural symmetry the through channel and the isolated channel can be exchanged for both versions A and B, with V_{b2} and V_{b3} exchanged accordingly.

V. Process and Fabrication

The fabrication of the PIN diodes has been summarized in Section II. The PIN diodes were life-tested for over 1600 hours at 275°C to determine their reliability. The PIN MMIC post isolation process was identical to the existing FET MMIC process [8]. All circuits on the wafer were dc probed during the processing. The wafers were thinned to 0.004 inch (100 micron), backside processed and then rf probed, scribed and separated into chip form.

The total yield of the chip processes including dc probe tests and visual inspection was higher than 80%. The rf on-wafer probing on those good devices (versions A and B) also showed a highly concentrated distribution of the S-parameters over 2–18 GHz. For insertion loss, more than 90% of the 1,115 rf probed devices were distributed within 0.2 dB of the average curve. Fig. 4(a) and 4(b) shows the layouts of versions A and B, respectively. Both circuits have the same size of 0.0685 × 0.140 inch (1.7 × 3.5 mm).

VI. Measurements and Performance

The fabricated PIN diode switches were measured in a three-port fixture for various tests. Both versions A and B exhibited similar rf test results, which will be shown later in Figs. 7 and 8, and both versions can be equally chosen based on the user's bias requirements. Thus no particular version will be specified hereinafter unless necessary. Fig. 5 shows the measured insertion loss versus simulated performance of a switch for both on-wafer and in-fixture cases. Agreement between data and models is excellent. The bias voltages were −8 V (3.7 mA) for the through channel and + 5 V (4.6 mA) for the isolated channel.

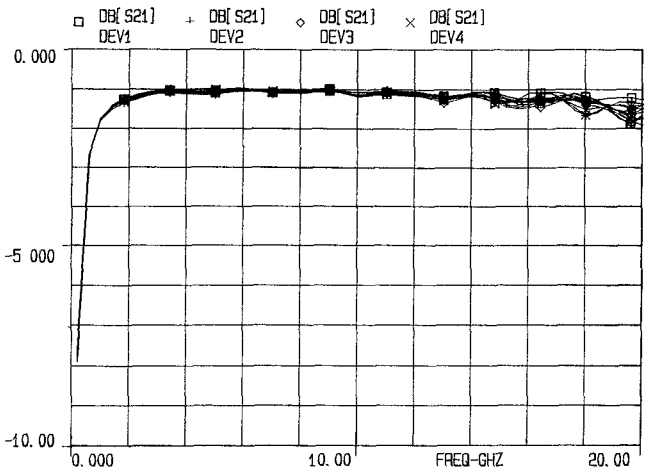


Fig. 7. Distribution of in-fixture measured insertion loss from seven switch samples (bias current = 3.7 mA).

In-fixture measured insertion loss was 1.15 dB with a peak ripple of 0.15 dB from 2–18 GHz. This loss level and flatness have not been reported before in a wideband switch incorporating on-chip bias networks [5]–[7]. The measured insertion loss improved slightly when higher bias current was applied. The input and output return losses, to be discussed in more detail later, were better than 12 dB. Fig. 6 shows the measured and modeled isolations of a switch, with isolation greater than 43 dB across the band. The agreement is better for the on-wafer case and for the low-isolation region.

To show the performance distribution, test results from seven samples (three version A and four version B) are superimposed in Fig. 7. The peak-to-peak spreading of the insertion loss is less than 0.2 dB up to 15 GHz and reaches 0.4 dB at 18 GHz. The isolation of the seven switches is greater than 42 dB, as shown in Fig. 8. These results reveal a very uniform performance of the insertion loss and the isolation of the switches.

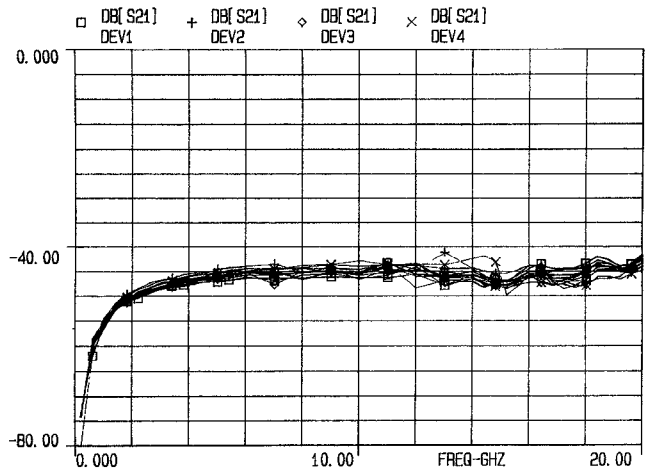


Fig. 8. Distribution of in-fixture measured isolation from seven switch samples (bias current = 3.7 mA).

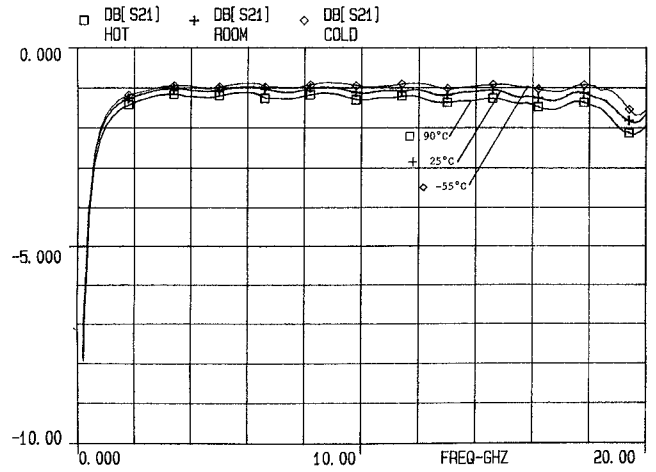


Fig. 9. Temperature variation of the insertion loss of a SPDT PIN diode switch.

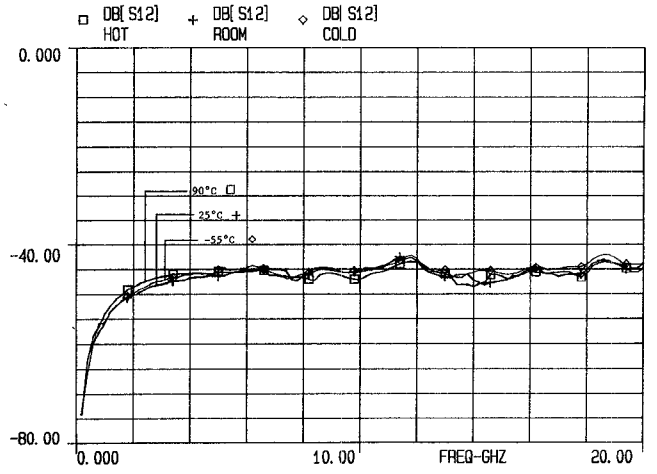


Fig. 10. Temperature variation of the isolation of a SPDT PIN diode switch.

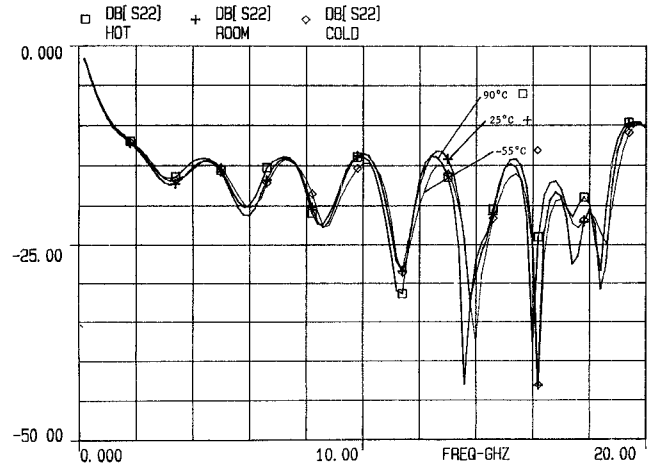


Fig. 11. Temperature variation of the output return loss of a SPDT PIN diode switch.

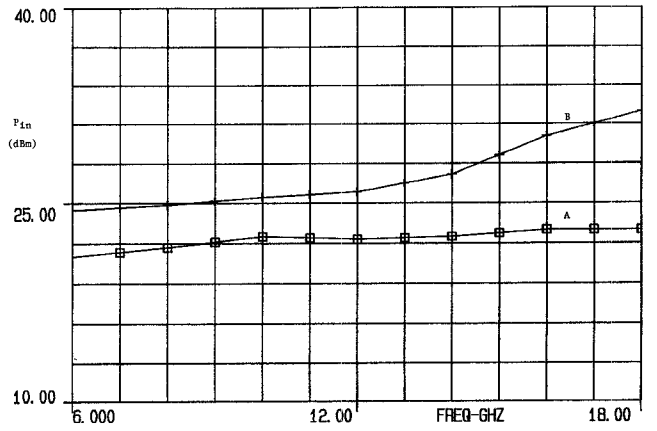


Fig. 12. Measured input power at 1-dB insertion-loss compression of a SPDT PIN diode switch. Bias voltage / current = −8 V / 3.7 mA (curve A) and −18 V / 9.3 mA (curve B).

On temperature sensitivity, two of the seven switches were tested across a −55°C to +90°C range. The insertion loss, isolation and return loss are shown in Figs. 9–11, respectively. It is seen that the insertion loss increases from about 1 to 1.5 dB with respect to the temperature increase, while the return loss and the isolation of the switches remain relatively insensitive to the temperature change. The higher insertion loss is believed to come from a higher diode resistances at elevated temperature. The low level ripples associated with the return loss in Fig. 11 are due to the parasitical coupling between the fixture's rf and dc feed lines in the non-ideal launchers.

The power handling capability of the switches depends on the bias voltages applied. A simplified expression for the input rf power rating, assuming that the diode's resistance is negligible compared to the bias resistance, is given by

$$P_{rms} = \frac{R_1^2 \mid V_{b12} \mid^2}{100(R_1 + R_2)^2} \tag{4}$$

The bias resistances R_1 and R_2 for the design are 800 and 1000 ohm, respectively. Nominal biases of $V_{b1} = 0$ V and $V_{b2} = -8$ V give $\mid V_{b12} \mid = 8$ V. Thus the approximate maximum rf input power from (4) is 23 dBm. The measured input power at the 1-dB insertion loss compression with the same biases is shown in Fig. 12 (curve A). It is seen that the measured curve approaches 23 dBm above 9 GHz. A higher bias of $V_{b2} = -18$ V (9.3 mA) raises the maximum power handling to about 31 dBm (1.25 W), as shown by curve B in Fig. 12. It should be noted that the power handling capability is controlled by the through channel biases rather than those of the isolated channel.

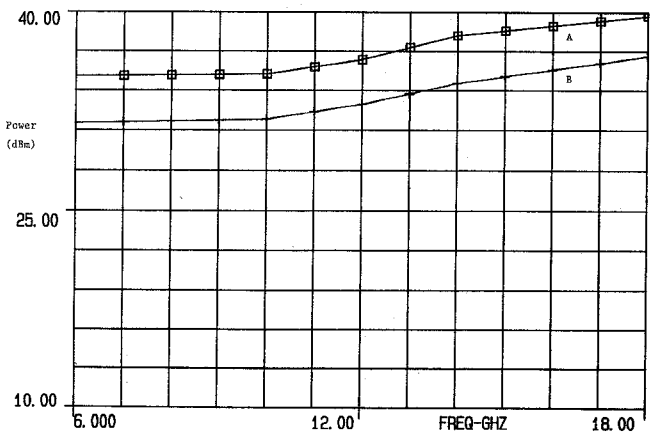


Fig. 13. Measured input power (curve A) and output power (curve B) in dBm at the third-order interception point of a SPDT PIN diode switch. Bias voltage / current = −8 V / 3.7 mA.

The input and output power of the switches at the third-order harmonic interception point, designated respectively as P_{in}(IP3) and P_{out}(IP3), were also measured at the nominal bias. The measured P_{in}(IP3) and P_{out}(IP3) in Fig. 13 reach almost 37 and 40 dBm, respectively, demonstrating a superior linearity of the devices. Fig. 13 also indicates that the linearity of the PIN diode switches improves with the increasing frequency, as opposed to a deteriorating linearity for MESFET switches [6], [9]. Measured spurious-free dynamic ranges [11] of these PIN diode switches vary from 77 dB at 6 GHz to 80 dB at 18 GHz.

VII. Conclusion

Two state-of-the-art PIN diode switches have been designed, fabricated and tested. These single-pole double-throw (SPDT) switches can be mass produced as monolithic GaAs IC's. Insertion loss over 2–18 GHz is 1.15 ± 0.15 dB, which is unprecedented in loss and flatness performance for monolithic wideband switches incorporating on-chip bias networks. Isolation and return loss are better than 43 dB and 12 dB, respectively. These performance characteristics have been measured at a nominal bias of −8 V, which corresponds to only 3.7 mA of series diode bias current. The total dc power consumption is 55 mW. The insertion loss is seen to be sensitive with respect to the temperature.

Excellent agreement in the insertion loss has been observed between the model simulations and the measurements. Input rf power at 1-dB compression of the insertion loss is 23 dBm when the bias of −8 V (3.7 mA) is used, which increases to 31 dBm at a higher bias of −18 V (9.3 mA). The input power of the switches at the third-order interception is 40 dBm, with a spurious-free dynamic range greater than 77 dB. Foundry production of these switches resulted in an overall final yield of more than 80%.

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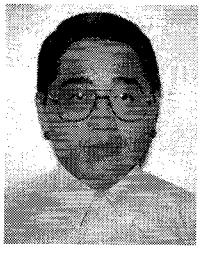

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Donna Zych, photograph and biography not available at the time of publication.

Elias Reese, photograph and biography not available at the time of publication.

Denis M. Drury, photograph and biography not available at the time of publication.